LIBRARY ieee ;

USE ieee.std\_logic\_1164.all ;

ENTITY lab6c IS

PORT ( w : IN STD\_LOGIC\_VECTOR(1 DOWNTO 0) ;

En : IN STD\_LOGIC ;

y : OUT STD\_LOGIC\_VECTOR(0 TO 3) ) ;

END lab6c ;

ARCHITECTURE Behavior OF lab6c IS

SIGNAL Enw : STD\_LOGIC\_VECTOR(2 DOWNTO 0) ;

BEGIN

Enw <= En & w ;

WITH Enw SELECT

y <= "1000" WHEN "100",

"0100" WHEN "101",

"0010" WHEN "110",

"0001" WHEN "111",

"0000" WHEN OTHERS ;

END Behavior ;